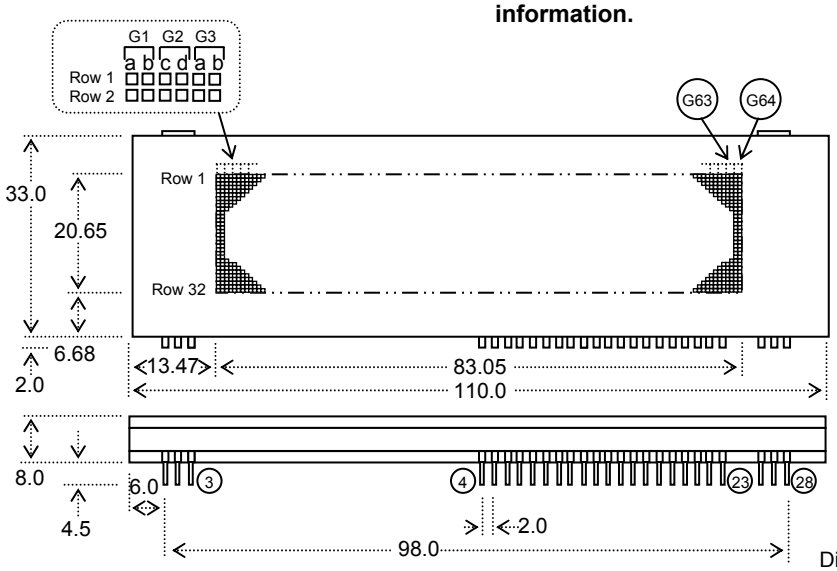
Graphic Dot Matrix Chip In Glass VFD MN12832JC

- **128 x 32 Graphic Dot Matrix**
- **Chip in Glass Driver IC**
- **High Brightness Blue Green Display**
- **Synchronous Serial Interface**
- **Low Pinout Count**
- **Wide Operating Temperature**

This VF glass includes 3 x 64 bit serial shift register, latched drivers which connect to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 50Hz to 60Hz. Consult our application notes for further information.



Dimensions in mm. See full spec for tolerances

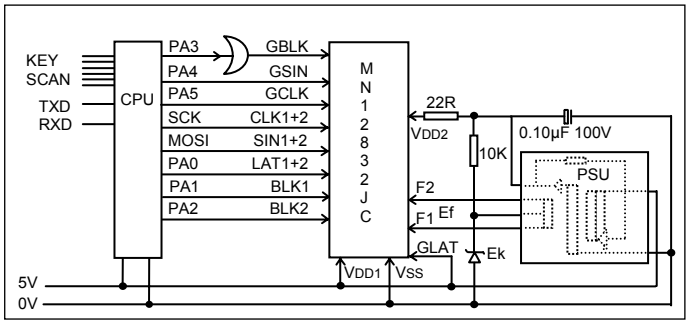
PIN OUT

Pin	Sig	Pin	Sig
1	F1	14	GBLK
2	F1	15	GLAT
3	F1	16	GCLK
4	BLK1	17	GSIN
5	LAT1	18	GSOUT
6	CLK1	19	NC
7	SIN1	20	SIN2
8	NC	21	CLK2
9	V_{DD2}	22	LAT2
10	V_{DD2}	23	BLK2
11	V_{SS}	26	F2
12	V_{SS}	27	F2
13	V_{DD1}	28	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	4.5	5.0	5.5	V	V_{SS}=0V
Logic Current	I_{DD1}	-	3.0	6.0	mA	V_{DD1}=5V
Filament Voltage	Ef	3.6	4.0	4.4	Vac	V_{DD2}=0V
Filament Current	If	180	200	220	mAac	V_{DD2}=0V
Display Voltage	V_{DD2}	50.0	60.0	63.0	V	V_{SS}=0V
Display Current	I_{DD2}	-	20.0	30.0	mA	V_{DD2}=60V
Filament Bias	E_K	-	5.0	-	V	V_{SS}=0V
Logic High Input	V_{IH}	$V_{DD1x0.8}$	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	0	-	+0.7	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	5.0	µA	V_{DD1}=5V
Logic Low Input	I_{IL}	-400	-250	-35	µA	V_{DD1}=5V

INTERFACE EXAMPLE

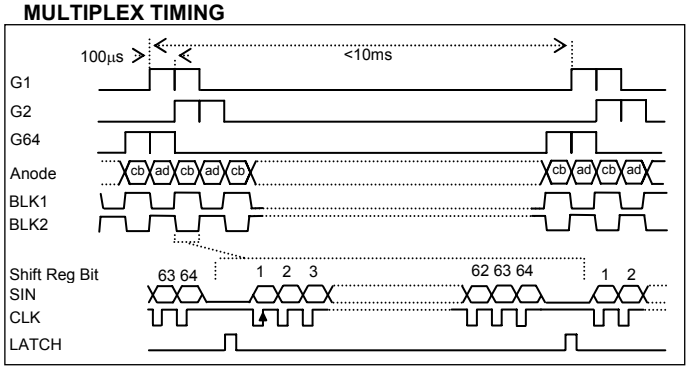


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	83.05 x 20.65
Dot Size/Pitch (XxY mm)	0.5 x 0.5/0.65 x 0.65
Luminance	600 cd/m^2 Typ.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. The 22R resistor at the V_{DD2} input is required to prevent current surge during switching.
3. If scanning of the display stops with V_{DD2} applied, the BLK input must be set high to prevent damage to the display.

MULTIPLEX TIMING



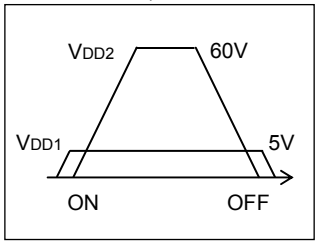
SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Grid G1-G64	GSIN1-64
Row 1 'ad'	SIN1 1,2
Row 1 'cb'	SIN2 1,2
Row 2 'ad'	SIN1 3,4
Row 2 'cb'	SIN2 3,4
:	:
Row 32 'ad'	SIN1 63,64
Row 32 'cb'	SIN2 63,64

INTERFACE TIMING

Parameter	Time
CLK Cycle	200ns min
CLK High	80ns min
CLK Low	80ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	5µs min

POWER SEQUENCE



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